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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,013	11/26/2001	James E. Jaussi	884.512US1	9548

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,013	JAUSSI ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in repose to the amendment filed 03/17/2003. Applicant's arguments are persuasive. The allowable subject matters of claims 6, 10-20, 22-26 and 28-30 have been withdrawn. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United Statcs and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 7-9, 21, 22 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwak et al. (US 2002/0039044) (newly cited).

As to claim 1, Kwak et al. discloses in figure 3 a current reference comprising: a current mirror circuit (140) to force a first current (I2) to be substantially equal to a second current (I1); a control transistor (Q10) coupled to the current mirror circuit to receive the first current, the control transistor having first and second bias terminals (gate and source) across which a bias voltage can be applied; a variable resistor (Q12) (the impedance of transistor 12 is varied in respond to the control voltage Vrefb. Therefore, transistor 12 is a variable resistor) coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current; and a control loop (120) to influence the biasing voltage.

As to claim 7, figure 3 shows the control transistor (Q10) comprises a NFET, and the first and second biasing terminals are a gate source of the NFET.

As to claim 8, figure 8 shows a second NFET (Q11) having drain terminal coupled to receive the second current from the current mirror, and having a source terminal coupled to provide the second current to the variable resistor.

As to claim 9, figure 3 shows a transistor (Q11) coupled drain-to-source between the current mirror and the variable resistor.

As to claim 21, figure 3 shows a current reference comprising a control transistor (Q10) having a gate terminal and source terminal; a variable resistor (Q12) coupled across the gate terminal and the source terminal of the control transistor, the variable resistor coupled receive a generated current; and control loop circuit (120) responsive to a current equal to the generated current, the control loop circuit coupled to influence the generated current.

As to claim 22, figure 3 shows a current mirror (140) coupled to the control transistor and the variable resistor.

As to claim 27, figure 3 shows an integrated circuit comprising: a control transistor (Q10) coupled in a first leg of a current reference circuit (140), the control transistor having first and second biasing terminals (gate and source); a variable resistor (Q12) coupled in a second leg of the current reference circuit and between the first and second biasing terminals of the control transistor; and a control loop circuit (120) to modify a resistance value of the variable resistor, the control loop circuit comprising a variable impedance output driver.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-5, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US 20020039044A1) in view of Kwan (USP 5949279A) (newly cited).

As to claim 2, Kwak et al.'s figure 3 shows all limitations of the claim except for the variable resistor comprises plurality of resistive devices in parallel. However, Kwan's figure 3 shows a variable resistor (101) comprises plurality of resistive devices (R1, T1-Rn, Tn) in parallel. Kwan's variable resistor in figure 3 having equivalent with the variable resistor (101) in figure 1. Figure 3 is a digital variable resistor and figure 1 is analog variable resistor. Therefore, it would have been obvious to one having ordinary skill in the art to modify Kwak's circuit by replacing the analog variable resistor (Q12) with a digital variable resistor (such as Kwan's figure 3) for the purpose of digitally control the current circuit. Thus, there will be a analog to digital converter that convert the output of circuit 120 to digital signal in order to digitally control the digital variable resistor.

As to claim 3, the modified Kwak shows the plurality of resistive devices having binary weighed values.

As to claim 4, the modified Kwak shows the plurality of resistive devices having control input node (gates of Kwan's T1-Tn) to enable the resistive device.

As to claim 5, the modified Kwak shows the control loop circuit (further included the newly added analog to digital converter (ADC)) includes output nodes (output of the ADC, and wherein the control input node of eah resistive device is coupled to one of the output nodes of the control loop circuit.

As to claim 23, the modified Kwak circuit shows the variable resistor comprises a plurality of variable resistance devices (Kwan's R1, T1-Rn, Tn) coupled in parallel, each of the plurality of variable resistance devices including an NFET responsive to the control loop circuit.

As to claim 26, the modified Kwak circuit shows a transistor (Q11) coupled to support a variable voltage between the current mirror and the variable resistor.

5. Claims 6, 24, 25 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US 20020039044A1) in view of Kwan (USP 5949279A) and in view of Burger, Jr. et al. (USP 6275090) (newly cited).

The combination of Kwak et al. circuit with Kwan circuit shows all limitations of the claim except for the control loop comprises a comparator and a state machine. However, Burger, Jr. et al. teaches in figure 1 a method for digitally controlling a reference circuit with feedback signals generated by feedback circuit (110 and 113). The feedback circuit comprising a comparator for comparing the output voltage with a reference voltage (VBG); an a state machine providing digital control signals in response to the output of the comparator. The feedback circuit is a simple analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art to employ Burger, Jr, et al.'s teaching to realize the modified Kwak circuit for the purpose of providing the digital control signals to control the variable resistor in response to the analog voltage.

6. Claims 10-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US 20020039044A1) in view of Kwan (USP 5949279A) and Burger, Jr. et al. (USP 6275090) and Perque et al (US 2002/0014914A1) (newly cited).

The combinations of Kwak et al., Kwan and Burger, Jr. et al references shows all limitations of the claims except for the control loop controlling plurality of similar current generating circuits. However, Perque et al. teaches in figure 5 that a control loop (11, R1 and R2) control plurality of similar current generating circuits (M1s and M3) for the purpose of providing plurality of similar current sources. Therefore, it would have been obvious to one having ordinary skill in the art to use the control loop in the modified Kwak circuit to control plurality of the current generating circuit similar to Kawk circuit 110 and Q13, with the digital variable resistor, for the purpose of providing plurality of current source circuits.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
April 17, 2003

Terry D. Cunningham
Primary Examiner